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Design and Implementation of Area Efficient Distributed Arithmetic using Divided LUT Architecture

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ABSTRACT

Digital filters are the essential units for digital signal processing systems. Traditionally, digital filters are achieved in Digital Signal Processor (DSP), but DSP-based solution cannot meet the high speed requirements in some applications for its sequential structure. Nowadays, Field Programmable Gate Array (FPGA) technology is widely used in digital signal processing area because FPGA-based solution can achieve high speed due to its parallel structure and configurable logic, which provides great flexibility and high reliability in the course of design and later maintenance. In general, Digital filters are divided into two categories, including Finite Impulse Response (FIR) and Infinite Impulse Response (IIR). And FIR filters are widely applied to a variety of digital signal processing areas for the virtues of providing linear phase and system stability.

Keywords –Distributed Arithmetic; FIR; pipeline; LUT; FPGA

Introduction

Digital filters are the essential units for digital signal processing systems. Traditionally, digital filters are achieved in Digital Signal Processor (DSP), but DSP-based solution cannot meet the high speed requirements in some applications for its sequential structure. Nowadays, Field Programmable Gate Array (FPGA) technology is widely used in digital signal processing area because FPGA-based solution can achieve high speed due to its parallel structure and configurable logic, which provides great flexibility and high reliability in the course of design and later maintenance. In general, Digital filters are divided into two categories, including Finite Impulse Response(FIR) and Infinite Impulse Response(IIR). And FIR filters are widely applied to a variety of digital signal processing areas for the virtues of providing linear phase and system stability.

The FPGA-based FIR filters using traditional direct arithmetic costs considerable multiply-and-accumulate (MAC) blocks with the augment of the filter order. However, according to Distributed Arithmetic, we can make a Look-Up-Table(LUT) to conserve the MAC values and callout the values according to the input data if necessary. Therefore, LUT can be created to take the place of MAC units so as to save the hardware resources.This paper provide the principles of Distributed Arithmetic, and introduce it into the FIR filters design, and then presents a 31-order FIR low-pass filter using Distributed Arithmetic, which save considerable MAC blocks to decrease the circuit scale, meanwhile, devided LUT metherd is used to decrease the required memory units and pipeline structure is also used to increase the system speed.

II. DISTRIBUTED ARITHMETIC

Distributed Arithmetic was first brought up by Croisier[1], and was extended to cover the signed data system by Liu , and then was introduced into FPGA design to save MAC blocks with the development of FPGA technology.

The N-length FIR filter can be described as:

$$y =< h,x >= \sum_{n=0}^{N-1} h[n]x[n]$$

Where h[n] is the filter coefficient and x[n] is the input sequence to be processed. The FIR structure consists of a series of multiplication and addition units, and consume N MAC blocks of FPGA, which are expensive in high speed system. Compared with traditional direct arithmetic, Distributed Arithmetic can save considerable hardware resources through using LUT to take the place of MAC units [2]. Another virtue of this method is that it can avoid system speed decrease with the increase of the input data bit width or the filter coefficient bit width, which can occur in traditional direct method and consume considerable hardware resources [3].

Distributed Arithmetic is introduced into the design of FIR filters as follows.

In the two's complement system, x[n] can be described as:

$$x[n] = -2^{B} x_B[n] + \sum_{b=0}^{B-1} 2^{b} x_b[n] \qquad (2)$$

Substituting equ.(2) into equ.(1) yields:

$$y = -2^{B} x_B[n]h[n] + \sum_{b=0}^{B-1} h[n] \sum_{n=0}^{N-1} 2^{b} x_b[n] \qquad (3$$

The second part of the equ. (3) can be changed into another form:

$$\sum_{b=0}^{B-1} h[n] \sum_{n=0}^{N-1} 2^{b} x_b[n] = \sum_{b=0}^{B-1} 2^{b} \sum_{n=0}^{N-1} h[n] x_b[n] \qquad (4)$$

Substituting equ. (4) into equ. (3) yields to the final form of Distributed Arithmetic:

$$y = -2^{B} x_B[n]h[n] + \sum_{b=0}^{B-1} 2^{b} \sum_{n=0}^{N-1} h[n] x_b[n] \qquad (5)$$

According to Distributed Arithmetic, we can make a Look-Up-Table(LUT) to conserve the MAC values and callout the values according to the input data if necessary. Therefore, LUT can be created to take the place of MAC units so as to save the hardware resources.

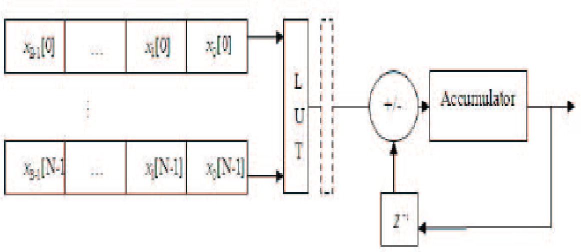

Fig.1 The basic Distributed Arithmetic structure

Look Up Table:

It stores the Filter co-efficient values.

As we are supposed to design 32-order filter, with the increase of filter order, the scale of LUT will increase dramatically [7], which will cost more time to look up the table and more memory to store the values. Therefore, we can divide the LUT unit into four small LUT units to solve this problem.

Coefficient values of small LUT is given below

Tab.2 Coefficient values of LUT

$b_3b_2b_1b_0$	Data
0000	0
0001	h[0]
0010	h[1]
0011	h[0]+ h[1]
0100	h[2]
0101	h[0]+ h[2]
0110	h[1]+ h[2]
0111	h[0] + h[1]+ h[2]
1000	h[3]
1001	h[0]+ h[3]
1010	h[1]+ h[3]
1011	h[0]+ h[1]+ h[3]
1100	h[2]+ h[3]
1101	h[0]+ h[2]+ h[3]
1110	h[1]+ h[2]+ h[3]
1111	h[0]+ h[1]+ h[2]+ h[3]

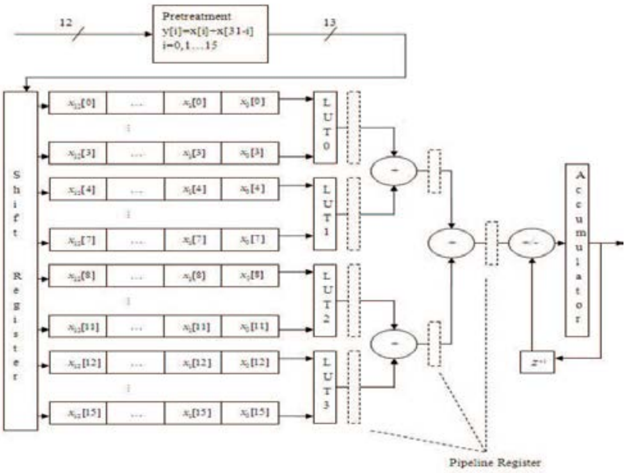

Fig: 2: Structure of FIR filter based on Distributed Arithmetic

The values of the four divided LUT units is added as the final value. The input data is defined as 12-bit-width complement, and the system can also process signed signals. According to the structure above, we achieve the whole design using Verilog language in Quartus 6.2, and the core code of the whole realization is as follows:

```
//P_DATA_W: processing bit width //shift_bit : to shift the data
//table_out_t: the output of the third leval register
//div_count: the number counter of system clock
if(div_count ==P_DATA_W-1)
sum<=sum – shift_bit (table_out_t, div_count-1); else
sum<=sum+shift_bit (table_out_t,div_count-1);
```

We also achieved the same filter using direct arithmetic to make a contract with the performance of the designed filter.

CONCLUSION

This paper presents the design and implementation based on Distributed Arithmetic, which is used to realize a 31-order FIR low-pass filter. Distributed Arithmetic structure is used to increase the resourse useage while pipeline structure is used to increase the system speed. The test results indicate that the designed filter using Distributed Arithmetic can work stable with high speed and can save almost 50 percent hardware resourses. Meanwhile, it is very easy to transplante the filter to other applications through modifying the order parameter or bit width and other parameters, and therefore have great practical applications in digit signal processing.

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