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A REVIEW PAPER ON HIGH SPEED ARITHMETIC LOGIC UNIT USING ROMs

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ABSTRACT

An ALU, adder and multiplication are the major component which defines the speed of an ALU. This paper deals with the construction of high speed multiplication using VHDL. Scientific application demand high floating performance for such requirement design of fast and efficient of arithmetic logic unit. In this simulation and implementation part, has been tested using Xilinx ISE 6.1i and ModelSim SE 5.5e synthesis tool. The best way to create FPGA and CLPD is via VHDL.

Keywords: Arithmetic and logic, FPGA, VHDL, Xilinx.

1. Introduction:-

1.1 Arithmetic logic unit (ALU)

An arithmetic logic unit (ALU) is a piece of computer memory (CPU) that carries out arithmetic and logic operations on computer learning tasks. In some embodiments, the ALU is divided into two parts namely arithmetic (AL) and logical (LU). ALU is the part of the computer that performs all arithmetic tasks such as logical evaluation, logistic regression and multiple comparisons. Scientific research and practice for high-performance steering requires high speed ALU and acceleration to reduce execution time.

1.2 Read only memory (ROM)

The ROM reads the predefined data it provides and allows us only read the data and make it possible for us to provide more detail, based on the purpose of the keep-in-place in which data is required. This ensures that the memory of the ROM is such that it stores the data forever,

1.3 Programmable logic device (PLD)

It has various combinational and sequential logic circuits are design using various logic gate and flip flop.

1.4 Field programmable gate arrays (FPGAs)

FPGAs are designed with the highest value of predefines and programmable interfaces to execute secure serial calls and I / Os add-ons. It is a simple game based on logical platforms and VLSI architecture built into a silicon section. FPGA cores are supported by their fast and different speeds.

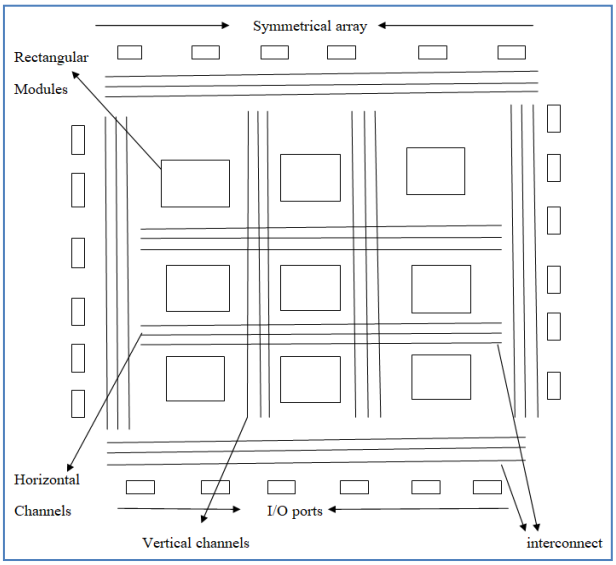

Figure 1: Diagram of FPGA

1.5 Complex programmable logic device (CLPD)

A Complex Programmable Logic Device (CPLD) is a combination of an entire program AND/OR an OR of a baby macrocells. In terms of AND / OR it is reprogrammable and can do a lot of reviews. Macrocells are the blocks that

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perform combinatorial logic or mode, and have the ability to change for real or coherent, with different response types.

2. Existing work on high speed ALU module

A new algorithm based design technique is suggested by Rita Mahajan, Gourav Saini assistant prof. focused on the high speed of ALU have been improves by using carry save adders and Radix 4-BOOTH multiplier. Its effect is compared by ripple carry adder and Vedic multiplier. BOOTH multiplier is faster than the Vedic multiplier. [1]

Rahul Sharma, Deepak Kumar introduced High-speed multiplier is designed and analyzed which is based on the algorithm named as "Urdhva Tiryakbhyam" sutra (UT Technique) which implemented on a VLSI chip. Employing UT techniques in the computation algorithms of the coprocessor will reduce the complexity, execution time, area etc. This method allows us to construct multiplier and practically saw that Proposed Vedic Multiplier is much more efficient than Array and Vedic multiplier. [2]

This paper deals the construction of high speed adder circuit using hardware description language (HDL) presented by Prashant Gurjar, Rashmi Solanki on the platform of Xilinx 9.2i and implemented on field programmable gate array (FPGA). In this paper have been simulated and synthesized various adders like full adder, ripple carry adder, carry-skip adder, carry select adder and carry-look ahead adder by using VHDL. The simulated results and performance of high speed adders and the parameters like area and speed analysis. This paper concludes that the carry-skip adder is more efficient in the speed and area consumption. [3]

Dharmana bhagavan introduced effort has been made to contrivance Arithmetic and logic unit, a random access memory (RAM) specific for 8 bit PIC microcontroller on field programmable gate array (FPGA) using VHDL as hardware description language. In this simulation, the code have been tested and verified using Xilinx 9.1i synthesis tool and also have a commercially available Xilinx 12.4i synthesis tool. It converts the number of the transfer link (RTL) into net level registers. [4]

Mr. Madhukar G Mrs. Akalpitha L Kulkarni Dr. J S Baligar shows the ASIC implementation of high speed and low power ALU. The ALU was designed for 16 bit integer data with four logic and four operations**.** The ALU was designed using the arithmetic circuits which have less power consumption and high speed. Hence the speed of the ALU was increased with low power consumption. [5]

Chandni N. Naika, Vaishnavi M. Velvania, Pooja J. Patela, Khushbu G. Parekh introduced that the ALU is one of the most important modules in a CPU and it can be modified during most instruction execution. In this paper 16 bit ALU is designed using VHDL and it is interfaced with RAM and ROM implemented in Xilinx. This 16-bit ALU will perform 15 different types of arithmetic, logical and shifting operations. [6]

Prof. Rajendra M. Rewatkar, Apurva V. Khole, Ashwini S. Kalinkar, Padmaja S. Banged, Shreya D Potey, presented the literature on designing of high speed, less area 64-bit ALU using efficient techniques. Parameters and area will be improved by using Carry Look Ahead Techniques and reduce the circuit complexity. The proposed design of ALU will performs the mathematical, logical and other operation. The ALU will be design using Xilinx software and simulation result will be verified on same platform using test benches. [7]

3. Methodology

BOOTH multiplier is the best technique in a high speed arithmetic logic unit. It's faster than the other techniques. It provides an efficient way of high speed arithmetic logic units using ROMs in this paper Wellance tree algorithm will be used to reduce the number of stages. By combine both BOOTH algorithm and Wellance Tree techniques both can be one multiplier. In high speed ALU ROMs will use 4-bit binary number.

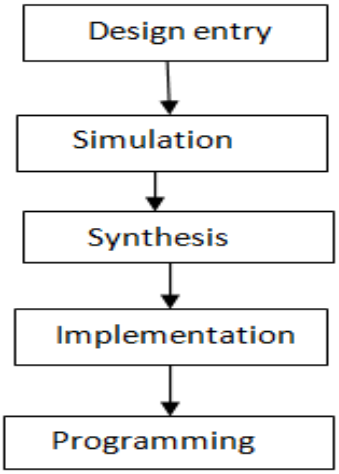

Figure 2: Design flow

Conclusion `

A design containing ALU using two ROMs both do addition and multiplication and also do subtraction and division. In this paper main focus is given on FPGA and CPLD for the high performance and speed of the circuit. The simulation work is done on Xilinx and ModelSim synthesis tool. VHDL code is used for the design of the circuit and verified separately on FPGA and CLPD.

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